Electronic Version
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Claims

[c1] 1. A method for fabricating a MOS transistor, comprising:
forming a gate dielectric layer on a substrate;
forming a first barrier layer on the gate dielectric layer;
forming an interlayer on the first barrier layer;
forming a work-function-dominating layer on the interlayer;
forming a second barrier layer on the work-function-dominating layer;
forming a poly-Si layer on the second barrier layer;
patterning the poly-Si layer, the second barrier layer, the work-function-dominating layer, the interlayer and the first barrier layer into a gate; and
forming a source/drain in the substrate beside the gate.

[c2] 2. The method according to claim 1, wherein forming the interlayer on the first barrier layer comprises performing a deposition process.

[c3] 3. The method according to claim 2, wherein the deposition process comprises a physical vapor deposition (PVD) process, an atomic layer deposition (ALD) process or a metal-organic chemical vapor deposition (MOCVD) pro-

cess.

[c4] 4. The method according to claim 1, wherein forming the interlayer on the first barrier layer comprises performing a surface treatment to the first barrier layer.

[c5] 5. The method according to claim 4, wherein the surface treatment comprises surface nitridation.

[c6] 6. The method according to claim 1, wherein forming the interlayer on the first barrier layer comprises performing a deposition process and a post-deposition surface treatment.

[c7] 7. The method according to claim 6, wherein the post-deposition surface treatment comprises surface nitridation.

[c8] 8. The method according to claim 1, wherein the interlayer is capable of controlling a crystal orientation of the work-function-dominating layer to adjust a work function of the work-function-dominating layer.

[c9] 9. The method according to claim 1, wherein the interlayer is capable of wetting a surface of the first barrier layer.

[c10] 10. The method according to claim 1, wherein a thickness of the interlayer is smaller than a thickness of the

work-function-dominating layer.

[c11] 11. The method according to claim 1, wherein a thickness of the work-function-dominating layer is larger than a total thickness of the first and second barrier layers.

[c12] 12. The method according to claim 1, wherein the gate dielectric layer comprises a high-K dielectric layer.

[c13] 13. The method according to claim 1, further comprising the following steps before the source/drain is formed:
forming a pair of lightly doped drains in the substrate beside the gate; and
forming a spacer on a sidewall of the gate,
wherein the spacer will serve as a mask together with the gate in the latter step of forming the source/drain.

[c14] 14. A MOS transistor, comprising:
a substrate;
a gate dielectric layer on the substrate;
a stacked gate on the gate dielectric layer, comprising, from bottom to top, a first barrier layer, an interlayer, a work-function-dominating layer, a second barrier layer and a poly-Si layer; and
a source/drain in the substrate beside the gate.

[c15] 15. The MOS transistor to claim 14, wherein the inter-

layer includes a material capable of controlling a crystal orientation of the work-function-dominating layer to adjust a work function of the work-function-dominating layer.

[c16] 16. The MOS transistor according to claim 14, wherein the interlayer includes a material capable of wetting a surface of the first barrier layer.

[c17] 17. The MOS transistor according to claim 14, wherein a thickness of the interlayer is smaller than a thickness of the work-function-dominating layer.

[c18] 18. The MOS transistor according to claim 14, wherein a thickness of the work-function-dominating layer is larger than a total thickness of the first and second barrier layers.

[c19] 19. The MOS transistor according to claim 14, wherein the gate dielectric layer comprises a high-K dielectric layer.

[c20] 20. The MOS transistor according to claim 14, further comprising:

a spacer on a sidewall of the gate; and

a pair of lightly doped drains in the substrate,

wherein the source/drain is in the substrate beside the spacer, and the lightly doped drains are in the substrate

beside the gate connecting with the source/drain.